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Welcome to the 2011 PCI Express® Solutions Resource Catalog

After an August release of the PCIe 3.0 specification for member review, the PCI Express community is eagerly awaiting the final specification by November. Anticipation is keen for a range of high-performance PCIe 3.0 products, especially in graphics, storage and networking applications, to hit the market within the year following spec completion. But as is typically the case, with performance improvements come design challenges.

Alex Goldhammer, strategic marketing manager for PCIe and Aurora at Xilinx, takes on this dichotomy in "PCIe: A Developer's Challenge; An Inventor's Enabler." And John Wiedemeier, product marketing manager at LeCroy, takes a cyclist's perspective to describe the test challenges involved in PCIe in "PCI Express Climbs to the Top."

EECatalog talked to Al Yanes, president and chairman of the PCI-SIG, and Nathan Brookwood, research fellow with Insight 64 and give you the benefit of their insight in "PCIe 3.0: The View Ahead." Finally, our virtual roundtable offers up opinions from chip, board and tool vendors on the trends and challenges they expect to face – and solve – as they help customers take advantage of the new standard.

As always, we'd love to hear your feedback, thoughts and comments. Send them to info@extensionmedia.com.

Cheryl Berglund Coupé

Editor

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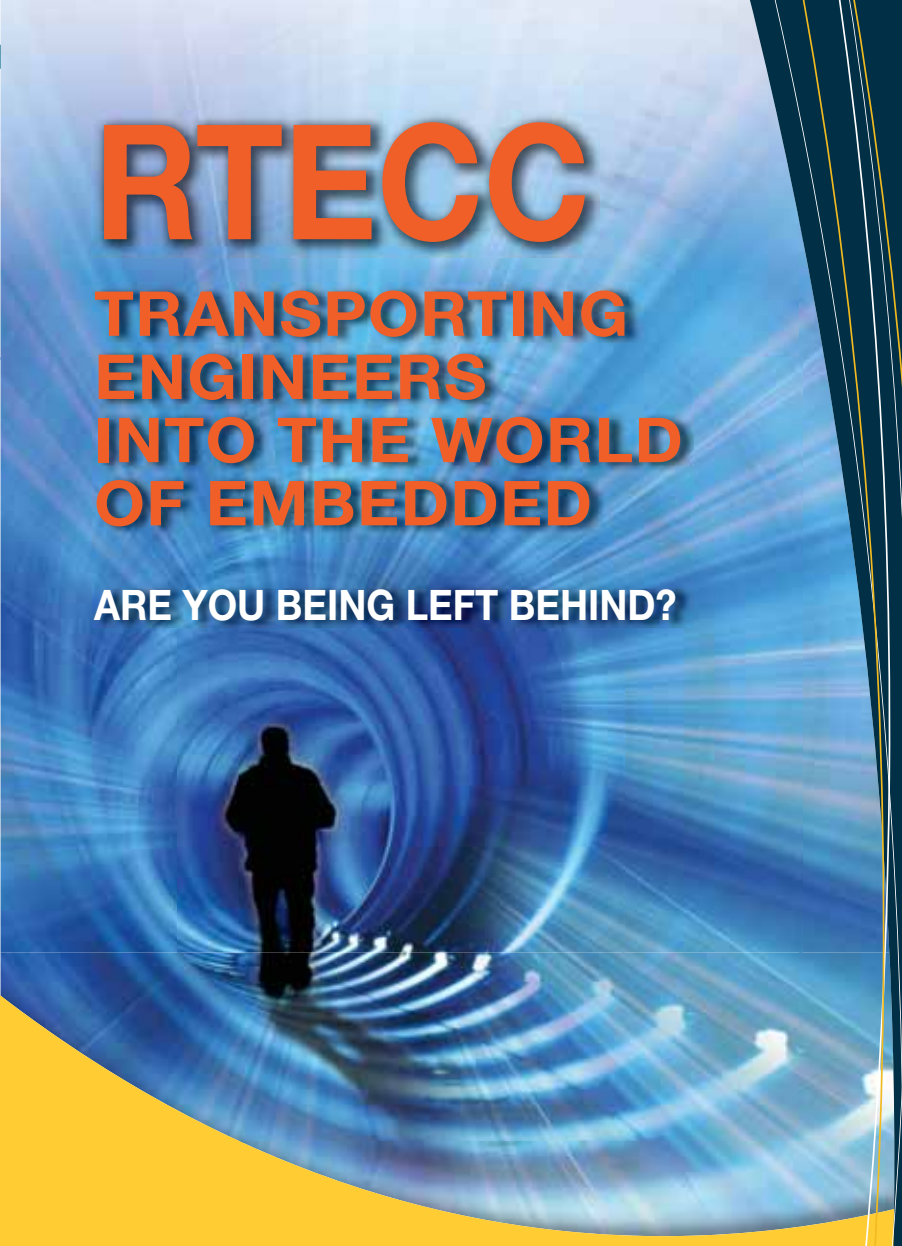

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PCIe 3.0: The View Ahead

Graphics, networking and storage applications stand to gain the greatest advantage with the new specification

By Cheryl Coupé

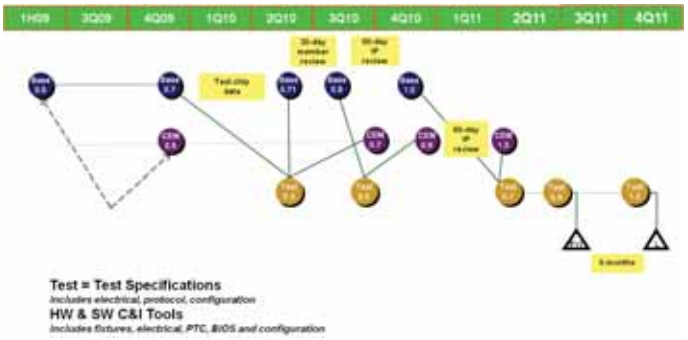
As it sits on the verge of announcing the PCI Express 3.0 specification (expected in November 2010), the PCI-SIG is looking forward to seeing products achieve new I/O bandwidth standards based on the technology. The group expects bandwidth evolution for the PCIe architecture will be driven primarily by graphics, Ethernet, Infinband, storage and PCIe switch applications – the current targets of the PCIe 3.0 technology.

	Raw Bit Rate	Link BW	BW/Lane/Way	Total BW x16
PCIe 1.x	2.5GT/s	2Gb/s	~250MB/s	~8GB/s
PCIe 2.x	5.0GT/s	4Gb/s	~500MB/s	~16GB/s
PCIe 3.0	8.0GT/s	8Gb/s	~1GB/s	~32GB/s

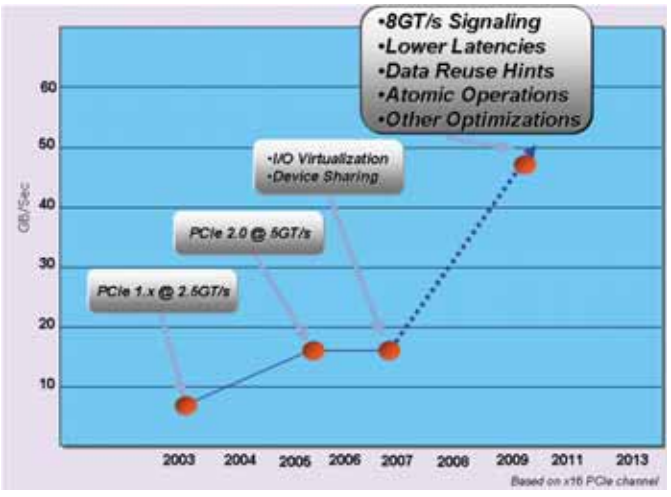
According to Insight 64 research fellow Nathan Brookwood, "PCI Express has already achieved near universality with regard to market acceptance, so the 3.0 extensions are more about allowing the standard to keep up with evolving requirements, rather than driving broader acceptance." Brookwood expects that PCIe 3.0 will ultimately impact client systems (desktops and workstations) with regard to graphics, and I/O-bound server systems. "The move toward cloud computing will exacerbate the I/O requirements for servers," he adds, "and may hasten acceptance of the new standard for these applications."

> **"PCI Express has already achieved near universality with regard to market acceptance."**

Brookwood explains that the PCIe 2.0 performance parameters were beginning to impact applications in three areas – graphics, networking and storage. As products incorporating the new standard go into commercial development, Brookwood believes the graphics segment will probably move first. "Consumers (who buy most of the high-end graphics cards) typically are less risk-averse than the corporate IT buyers who acquire most of the high-end networking and storage systems," he states. "Of course, users won't be able to realize any of these performance benefits until the chip and system suppliers add PCIe 3.0 support to their CPUs and systems, and the GPU, storage and network controller companies update their products for the new standard. This process will take at least two years."



PCI-SIG President Al Yanes agrees that desktop and server products will continue to embrace PCI Express for I/O bandwidth needs, and he sees opportunities to evolve the standard in the future for both the high-bandwidth, high-power I/O space, and the low-bandwidth, low-power space.



"Bandwidth evolution for the PCIe architecture will be driven primarily by graphics, Ethernet, Infinband, storage and PCIe switch applications."

At the same time, Yanes sees continued opportunities for previous generations of the PCIe standard. "PCI Express provides backward compatibility, so older products, or those not requiring I/O bandwidth improvements, may choose to implement PCI Express 1.0 or 2.0 architecture."

Al Yanes has served as president of the PCI-SIG since 2003 and chairman since 2006 and is a Distinguished Engineer for IBM in the Systems & Technology Division. He has 26 years of experience working with ASIC design in the I/O industry. Yanes holds 25 patents for PC I and other I/O technologies. Yanes is a PCIe technology expert for the IBM Rochester office and he is involved in IO design for IBM's Server products. Yanes holds a B.S. in computer engineering from Rensselaer Polytechnic Institute.

Nathan Brookwood has participated in the information technology industry since the days of the first transistorized computers. In 1998 he established Insight 64, where he serves as the research fellow, concentrating on CPUs and GPUs used in general purpose computing applications.

Feel the Need for Speed?

PCI Express performance enhancements offer tradeoffs for increased complexity

By Cheryl Coupé

With the final PCIe 3.0 specification due in November 2010, tool, board and chip vendors are working hard to conquer the new spec's complexities in order to take advantage of its performance enhancements. John Wiedemeier, product marketing manager at LeCroy; Alex Goldhammer, strategic marketing manager for PCIe and Aurora at Xilinx; and Patrick Dietrich, hardware design engineer at Connect Tech, discussed trends to watch and challenges to watch out for in our virtual roundtable discussion.

EECatalog: What major trends within engineering for PCI Express are you and your colleagues spotting?

John Wiedemeier, LeCroy: There are three protocol levels of PCI Express – Gen 1, Gen 2, and Gen 3 – and we're tracking each of these separately. Even with new standards, the old ones are still very much in force and people are still moving towards those from other technologies. We're still seeing people move from PCI to PCI Express, and we're still seeing embedded applications moving away from proprietary backplanes to Gen 1 and Gen 2 PCI Express backplanes. Servers are the major adopters for PCIe 3.0; workstations and graphics are the major adopters for PCIe 2.0; embedded is still moving from PCI to PCIe 1.1. People are using the I/O technology as a differentiator against their competition. Companies that are really sensitive to that, like graphics cards and servers, they'll be our first adopters for the higher speed technology.

Patrick Dietrich, Connect Tech: We are seeing PCI Express being used for more interchip communications. A perfect example is the new Intel Atom architecture. Normally, between processor and chipset there is a proprietary bus. The new architecture uses PCI Express between processor and chipset. This is great because there is already a robust knowledge of the specification throughout designers.

Alex Goldhammer, Xilinx: With PCI Express Gen 2 and USB 3.0, both protocols used the Intel PIPE 2.0 specification as the basis for the internal interface between the Protocol Layers and the GT (PHY). From a GT development perspective, this should help engineering reuse a lot of the verification and testing infrastructure needed for transceivers. If this trend continues it will also hopefully reduce the numbers of different transceivers in the market, making transceivers easier to test and validate. There will always be many, but efforts to consolidate will help.

EECatalog: What major challenges are your developers confronting these days?

Wiedemeier: Dynamic equalization will be a challenge for PCI Express Gen 3. Gen 1 and Gen 2 technologies use the same encoding protocol, and just increased the speed and performance characteristics. But when they went to Gen 3, they really changed the protocol drastically. One of the ways is with dynamic equalization. Right now, no one has that in place – they're using manual equalization to define the lanes up front.

> ***"Measuring and verifying PCI Express is becoming more and more difficult as the bus speed increases."***

Another trend that was really hyped at the Intel Developer Forum was solid state drive (SSD) devices, and SSD debugging will be another challenge.

Dietrich: Measuring and verifying PCI Express is becoming more and more difficult as the bus speed increases. Generation 2 at 5 Gbps pushes the bandwidth of our current oscilloscope and measurement equipment. With Generation 3 at 8 Gbps, our current equipment will not be able to measure it accurately. This will push design teams into making big investments in new equipment.

Goldhammer: The major challenge in PCI Express is the constant doubling of speed/bandwidth. At each generation the internal data path must also double; there is a tremendous amount of complexity involved in keeping the cores efficient and physically small. Most of this work is just brute force, but there are also demands to reduce latency and add new capabilities such as some of the optional ECNs (Engineering Change Notices) released by the PCI-SIG and demanded by customers and enabled by Intel and other host processors.

Also with each new generation, the link training and state machines get increasingly complex. The link training is the automatic mechanism where link partners negotiate lane widths and lane speeds; these operate autonomously (without need for user intervention) and must be extremely robust. Xilinx uses Bus Functional Models (BFMs) in verification, but also uses released generations of FPGAs and boards to prototype and test in real hardware the behaviors of the transceivers.

> ***"PCIe-based SSD technology is going to change the whole storage environment."***

Lastly, as the data rates increased to 8Gbps for PCIe Gen3, the encoding has also changed to 128b/130b with scrambling. This is a non-industry standard encoding compared to 8b/10b, so this has created a lot of additional work and complexity to switch between encoding.

EECatalog: How are you planning to leverage PCI Express 3.0?

Wiedemeier: LeCroy is providing a PCIe 3.0 protocol analyzer and exerciser to help early adopters to be ready for the PCIe 3.0 v1 spec release at the end of the year. Our exerciser allows developers to get started testing with PCIe 3.0 host or device before PDKs are available.

Dietrich: Most of our products currently do not need the features that PCI Express 3.0 brings, such as CPU carrier boards, digital I/O, multi-port serial, etc. However, we are looking forward to the next generation of PCI Express for our FPGA/DSP based products which require high-speed and high bandwidth properties where approximately1GB/s per lane can be used.

Goldhammer: With PCIe 3.0, Xilinx is continuing to track very closely with the PCI-SIG release schedule and Intel's roadmap for deployment. Since the specification for 3.0 is expected to be finalized by the end of the year, Xilinx is going to be using a combination of soft IP and integrated blocks to support PCIe Gen3 in Kintex-7 and Virtex-7 families.

In the market, PCIe has proliferated into pretty much all market segments, hence Xilinx integration of PCIe hard blocks in all FPGAs with transceivers. For PCIe Gen3, we see multi-10 Gigabit Ethernet and 40 Gigabit Ethernet as the main drivers of PCIe bandwidth. 100 Gigabit Ethernet is also driving PCIe bandwidth needs. Image processing is another key driver for PCIe 3.0. Whether medical imaging, 3D TV or HDTV, video applications take advantage of FPGA processing capabilities and high-speed PCIe ports. High-performance computing (HPC) in applications like oil and gas exploration and financial applications are the other key areas where the demand for more PCIe bandwidth and high-performance is almost insatiable.

EECatalog: What new, leading- and bleeding-edge technologies are you most excited about?

Wiedemeier: PCIe-based SSD technology is going to change the whole storage environment.

Goldhammer: In PCIe, Active-State Power Management (ASPM) is a capability where links can automatically go in and out of low-power states to save system-level power. ASPM has run into bumps in the road due to complexity and challenges in the definition. Power is a major system concern in the market. Xilinx is an advocate of power-saving technologies and is excited to see how the industry continues to adopt these optional power-savings capabilities into PCIe devices.

Virtualization is another area we are excited to see opening up. Single-Root I/IO Virtualization (SR-IOV) has been rolled out in servers already, but the rest of the industry is also coming up to speed. As cloud computing becomes more pervasive, this technology will be critical to its success.

Cheryl Berglund Coupé is Editor of EECatalog.com. Her articles have appeared in EE Times, Electronic Business, Microsoft Embedded Review and Windows Developer's Journal and she has developed presentations for the Embedded Systems Conference and ICSPAT. She has held a variety of production, technical marketing and writing positions within technology companies and agencies in the Northwest.

PCI Express Climbs to the Top

By John Wiedemeier, LeCroy Corporation

Producing the next generation tools for PCI Express Developers feels like working in the pit for the cyclists in the Tour de France competition. Over the last few years, test tool requirements have become more stringent and their necessity to projects has been the difference between success and failure. PCI Express is moving in many directions and it is very challenging to anticipate where it will head next.

PCI Express 3.0 Development

The climb to PCIe 3.0 is in low gear now. Many companies are finding themselves ascending steeper development slopes than originally imagined. Issues such as dynamic equalization and protocol specification adherence make this a treacherous path. The PCI Express 3.0 specification, first announced in 2008, described a new data rate of 8GT/s and a new encoding format of 128b/130b – all of this while maintaining backwards compatibility with the legacy Gen1 and Gen2 versions of the same protocol. Dynamic equalization, a link initialization process where training sequences communicate transmitter and receiver parameters to establish a link, has been especially difficult. New structures added to the physical layer, such as sync header bits, protocol level start tokens for TLPs and DLLPs, data block streaming and more, require developers to stop and figure out how these changes affect their products.

Fixing problems related to this new protocol structure, higher speeds and dynamic equalization in the pre-silicon period of development is crucial. One way to insure that this is possible is by having the same debugging tool and interface for pre-silicon as in the post-silicon development phase. Many post-silicon tools are more robust and better suited to interoperability debugging. In some cases, it is even necessary to combine digital tools with analog tools. For example, a good way to find issues that deal with dynamic equalization are if both analog waveforms and high level protocol packets are synchronized together with the protocol packet view used to navigate to hard-to-find details of dynamic equalization. Developers seeking to solve this problem should look to their tool vendor for a full range of tools that address both the analog and digital layers of the protocol.

This trace of a NVMHCI SSD application taken with the LeCroy Summit T3-16 Protocol Analyzer shows a decoded SSD NVMHCI 1.0 packet.

What about Gen1 and Gen2?

Although PCI Express 3.0 is the new technology being adopted by high-performance products such as servers and high-speed I/O add-in cards, the PCI Express 1.0 and 2.0 technologies are still moving forward. Over the last several years many applications have moved from legacy PCI to PCI Express 1.0. This has been true in the embedded board markets that serve the military, telecommunications and industrial markets. Standards such as the VITA 46, VITA 42, and AMC.1 R2.0 have started to feature PCI Express I/O. Almost all new embedded board form factor specifications announced in the last few years have PCI Express support on them. VPX backplanes, AMC, and XMC mezzanine module base applications are moving from PCIe 1.0 to 2.0. Interoperability between various system components is a serious problem that is being addressed through tried and proven tools coming from the PC/server industry.

> ***"Over the last few years, test tool requirements have become more stringent and their necessity to projects has been the difference between success and failure."***

One of these embedded technologies that is revolutionizing embedded platforms is the VPX specification – also known as VITA 46 – developed by VITA (VME International Trade Association). It is a next-generation VMEbus-based system that offers support for switched fabrics such as PCI Express over a new high-speed connector. Defense and aerospace systems are the primary focus with a wide range of target applications including graphics, mass storage and switches.

Debugging embedded systems sometimes presents a probing challenge to engineers, such as how to take tools used in mainstream PC/servers and apply them to fix similar issues in the embedded environment. Test equipment that readily connects to PC or server boards may not be suitable for a ruggedized backplane. Connectivity to the device under test must be solved before test equipment can be deployed to solve problems. Embedded systems engineers depend on test equipment to be flexible to work in various applications in order to maximize debugging capability.

Laptop and Graphics Computing

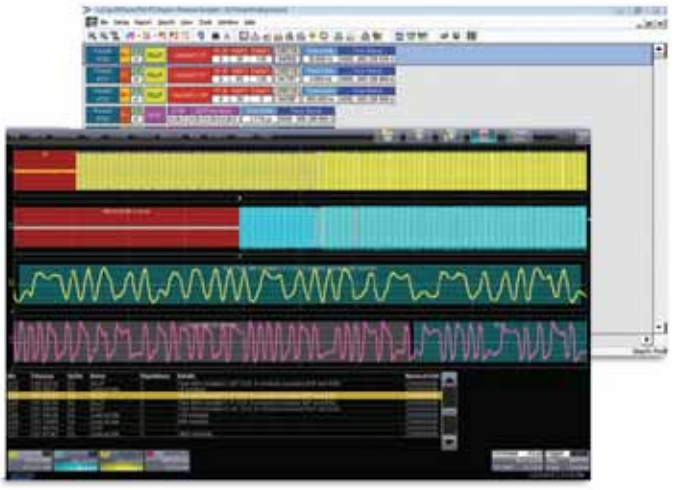
PCIe 2.0 has been the new focus of graphics card performance and laptop computing. All graphics card manufacturers include a high performance PCI Express 2.0-featured graphics card in their product line. Differentiation in performance between vendors is determined by how well the PCIe flow control buffer is managed and how host-to-device packet efficiency is achieved. Tuning this performance has become essential to competing in this market.

Laptop computers use small form factor modules like PCI Express Minicard 2.0 and ExpressCard 2.0. Each of these modules help users and manufacturers to upgrade the feature set of the laptop. The Mini Card Electromechanical Specification Revision 1.2, developed by the PCI-SIG®, defines a small form-factor I/O card with a high-speed connector that supports primarily PCI Express. Mini Card applications include 802.11x wireless adapters, Bluetooth interfaces, Ethernet adapters, modems, solid state drive (SSD) modules and SATA storage. Laptop vendors have enabled a flexible user upgradability option through the new ExpressCard 2.0 standard developed by the PCMCIA. This specification is now part of the USB-IF portfolio, and is a small form-factor mobile I/O card running at data rates up to 5 GT/s to support primarily PCI Express 2.0. ExpressCard applications can include expanded system interfaces, storage and multimedia devices such as wireless, SATA drives and SSD modules. Decisions about how to best test laptop modules like these usually go in two directions: Testing in laptop and testing out of laptop. Having flexible test fixtures can give the developer the best of both worlds.

PCI Express Extensions

Server I/O – once limited to how many slots in its chassis – now has the option to expand its I/O size through the PCI Express External Cabling Specification, developed by the PCI-SIG®. This high-speed cabling interface is used for local networking and PCIe bus expansion. Applications include split systems where there are remotely connected I/O controllers, I/O expansion that connects different types of I/O form factor cards to a system, server I/O expansion card connectivity, and connecting external graphic systems. Like any distanced connection, jitter and protocol synchronization are required to establish good signal transmission.

"New protocol tools that provide understandable user views by abstracting the complex register operation make a big difference in solving problems and meeting time-to-market requirements."



This trace of a PCIe 1.0 application taken with a LeCroy Oscilloscope using the Protosync PE application shows how physical layer information can be synchronized with high-level digital packet information.

Solid state drives are now becoming more popular. The storage industry is working to create the NVMHCI server specification that will enable better guidelines for how PCIe-based SSD devices are developed and supported in server environments. Although a consumer specification is available today, many expect the server specification to encompass both consumer and server needs. The difficulty of using indirect register schemes to manage storage communication has been a barrier to new competition in this market. New protocol tools that provide understandable user views by abstracting the complex register operation make a big difference in solving problems and meeting time-to-market requirements. The storage industry is highly interested in SSD technology for several reasons, including faster data access, increased longevity and reliability, less noise, non-volatile storage, and less maintenance of failing hard drives.

Conquering the Course

Development projects based on PCIe 1.0 to 3.0 that used tools like protocol analyzers and exercisers saw a big difference in meeting product schedules. The key factor in deciding to use this type of equipment for most engineers is that highly complex digital serial transmissions can be rendered into simple-to-understand information and verified against the PCI Express specification. Once the slopes of protocol interpretation and verification are conquered the course to debugging is fairly straightforward.

John Wiedemeier is the senior product marketing manager responsible for interconnect testing technologies at LeCroy Corporation, where he has managed the PCI Express protocol analyzer/exerciser product lines. He has 22 years experience in the computer and embedded development industries. John is a member of the PCI SIG where he serves as a member of the PCI Express Serial Enabling Work Group. John is also a member of the PICMG and VITA organizations promoting test strategies for AMC and XMC mezzanine cards. He has a BS in electronics engineering from Brigham Young University.

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http://eecatalog.com/pcie
Comprehensive technology information for engineers, designers, embedded developers and managers using or considering PCI Express.

http://www.pcisig.com/specifications/pciexpress/
Standards development group. Offers details of technology specifications, document review and compliance testing, test software and checklists

http://en.wikipedia.org/wiki/PCI_Express
From Wikipedia, the free encyclopedia. PCI Express (Peripheral Component Interconnect Express), officially abbreviated as PCIe (or PCI-E, as it is commonly called), is a computer expansion card standard designed to replace the older PCI, PCI-X, and AGP standards.

http://www.intel.com/technology/pciexpress/devnet/
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http://4gworld.com/

ESC Silicon Valley
San Jose, CA
May 2-5, 2011
http://esc-sv09.techinsightsevents.com/

TIA 2011: Inside the Network
May 17-20, 2011 - Dallas, TX
http://www.tia2011.org/

PCI-SIG Developers Conference
June 2011
http://www.pcisig.com/events/devcon_10/

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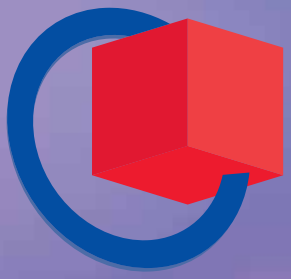

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NÜRNBERG MESSE

PLX Technology

ExpressLane™ PCI Express 3.0/2.0/1.x

OS Support: Windows, Linux, Others

Bus Interface: PCIe

PLX Technology (NASDAQ: PLXT), a leading global supplier of software-enriched silicon connectivity solutions for the enterprise and consumer markets, offers the industry's broadest portfolio of PCI Express Switches and Bridges. With a rich history of leadership in PCIe, PLX has been first to market across all families and carries the lowest power, lowest latency, and unmatched feature-set of any supplier.

With PCI Express 3.0 switches now available and encouraged for all new designs, PLX also has a rich catalog of 1.0a, 1.1, and 2.0 Switches and PCI and PCIe Bridges ready to ship today. Ranging from 4 to 96 lanes, PLX has the right configuration for your design.

Designers should also take notice of PLX's other industry leading families including 10GBase-T PHY (Teranetics), USB 3.0/2.0/1.0 controllers (NetChip), as well as our NAS and DAS consumer storage SoCs and controllers (Oxford).

Visit plxtech.com for information.

FEATURES & BENEFITS

- ExpressLane PCI Express 1.0/2.0/3.0 Switch Family includes high performance, low latency, low power, multipurpose, highly flexible and highly configurable devices
- ExpressLane PCI Express Bridges provide forward and reverse bridging. Our PCIe Bridge family allows designers to migrate local bus, PCI and PCI-X bus interfaces to the serial, PCIe Architecture
- PLX's Teranetics 10GBase-T PHY family is the industry's first single-chip implementation of single-port and dual-port 10GBase-T PHYs. Now sampling 40nm solutions
- PLX is the leader in high-performance consumer direct attached storage (DAS) and network attached storage (NAS) controllers
- PLX USB controllers are widely used in printers, portable media players, GPS systems, TV tuners, PCs, laptops, notebooks, WLAN devices, mobile phones, digital cameras and camcorders

AVAILABILITY

All products shipping today

APPLICATION AREAS

Data Center and Cloud Computing, Graphics, Industrial, Embedded, Consumer

CONTACT INFORMATION

PLX Technology, Inc
870 W. Maude Ave
Sunnyvale, CA 94085
USA
plxtech.com

ExpressLane™ PCI Express 3.0 Switches

OS Support: Windows, Linux, Others

Bus Interface: PCIe

The new innovative PLX® ExpressLane™ PCIe Gen 3 switch family, designed on 40nm process node, includes broad lane counts ranging from 12 up to 48 lanes. Board and system designers can take full advantage of the latest PCIe specification—8 Gbps in both directions (Tx/Rx), per lane—thus enabling one PLX 48-lane Gen 3 switch to handle an astounding 96 Gbps of full peer-to-peer bandwidth. PLX's Gen 3 switches also offer hot-plug controllers, virtual channels, and a non-transparent (NT) port feature, which enables the implementation of multi-host systems in communications, storage, and blade server applications.

PLX PCIe Gen 3 switches include exclusive software driven on-chip hardware debug and monitoring features such as measurement of the SerDes eye inside the device; PCIe packet generation to saturate x16 Gen 3 port; injection of error in live traffic; error logging; port utilization count; as well as PCIe and traffic monitoring for easy bring-up of PCIe systems that would otherwise require days of lab set-up and hundreds of thousands of dollars in test and measurement equipment. Furthermore, PLX offers designers a software development kit that simplifies design-in of the switch and its value-added features.

FEATURES & BENEFITS

- PEX 8748: 48 lane, 12 ports and PEX 8747: 48 lane, 5 ports
- PEX 8732: 32 lane, 12 ports
- PEX 8724: 24 lane, 6 ports
- PEX 8716: 16 lane, 4 ports
- PEX 8712: 12 lanes, 3 ports

TECHNICAL SPECS

- Highly Flexible Port Configurations
- Lowest Power and Lowest Latency
- Non-Transparent Port Capability
- True Peer-to-Peer Data Transfer
- Hot-Plug Support

AVAILABILITY

Sampling November 2010, Production mid-2011

APPLICATION AREAS

Data Center and Cloud Computing, Graphics, Industrial, Embedded

CONTACT INFORMATION

PLX TECHNOLOGY®

PLX Technology, Inc
870 W. Maude Ave
Sunnyvale, CA 94085
USA
plxtech.com/pcie

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Xilinx Solutions for PCI Express

Supported PCI Express Standards: Versions 1.1 and 2.0
OS Support: Windows and Linux
Bus Interface: PCI Express

Xilinx® solutions for PCI Express® enable designers to meet the most demanding bandwidth, power, and cost requirements for developing systems compliant with the widely adopted serial interconnect standard.

These solutions are enabled by the Xilinx integrated blocks for PCI Express in both the high performance Virtex® and low-cost Spartan® FPGA series. In the latest generation Virtex-6 and Spartan-6 devices, configurable PCIe blocks are implemented with built-in high-speed serial transceivers to save valuable logic resources and power, while delivering cost-effective features, performance, and programmability.

PCI Express designs can be up and running right out-of-the-box with Xilinx connectivity development kits. As part of the Xilinx Connectivity Targeted Design Platform, these flexible, scalable kits provide hardware, software tools, IP, customizable reference designs, and PCI Express form-factor cards to jump-start development, integration, and debug of system interfaces for a wide range of chip-to-chip, backplane, and box-to-box applications.

FEATURES & BENEFITS

- Virtex-6 FPGA PCI Express blocks support x1, x2, x4 and x8 Gen1 (2.5Gbps) and Gen2 (5Gbps) interfaces
- Virtex-6 FPGA GTX transceivers enable up to 6.5Gbps with industry's best signal integrity and eight programmable levels of Transmit Pre-emphasis and four programmable levels of Receive Equalization
- Spartan-6 FPGA PCI Express block supports x1 Gen1 (2.5Gbps) interfaces with less than half the power of previous generations
- Spartan-6 FPGA GTP transceivers enable up to 3.125Gbps with programmable Transmit Pre-emphasis and Receive Equalization

TECHNICAL SPECS

- Virtex-6 FPGA and Spartan-6 FPGA Connectivity Kits
- Virtex-5 FPGA Development Kit for PCI Express
- Spartan-3 FPGA PCI Express Starter Kit

AVAILABILITY

Virtex-5 FPGA and Spartan-3 FPGA PCI Express kits available now.

To learn more, visit http://www.xilinx.com/kits.

APPLICATION AREAS

Automotive, Aerospace and Defense, Broadcast, Consumer Electronics, Wired and Wireless Communications, as well as Industrial, Scientific and Medical Instrumentation

CONTACT INFORMATION

XILINX

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2100 Logic Drive
San Jose, CA 95124-3400
USA
408-559-7778 Telephone
more_info@xilinx.com
www.xilinx.com/connectivity

PLDA

Win the Race to PCIe Gen3 with PLDA IP Solutions

OS Support: Windows and Linux

Bus Interface: PCI Express

PLDA PCI Express 3.0 IP for ASIC and FPGA provides full PCIe Gen 3 functionality from the trusted leader in PCIe IP solutions. PLDA has over 15 years of design experience with PCI interfaces, ensuring first-time-right design success. PLDA's PCIe Gen 3 IP solutions provide:

- Seamless ASIC and FPGA integration, allowing you to design for FPGA and painlessly port to ASIC
- A broad range of user interfaces to answer simple to more complex design requirements
- Quick and reliable customization to ensure the IP will fit your specific needs
- A free evaluation program that includes the same deliverables and technical support as the licensed IP
- Industry-acclaimed technical support provided by the IP team

TECHNICAL SPECS

- PCIe IP core in synthesizable Verilog RTL encrypted or clear source code, compliant with the PCIe Base 3.0 Draft Specification, rev.0.9
- Supports Gen3 (8.0 GT/sec), Gen2 (5.0 GT/sec) and Gen1 (2.5 GT/sec) speeds at x1, x2, x4 and x8 lanes withfull backwards compatibility
- PIPE 3.0 interface to FPGA PHY/transceivers at 32-bit/250Mhz in Gen3 mode
- Multiple user interface options including Transmit/receive (Tx/Rx), Transaction Layer bypass, EZDMA multi-channel DMA and AMBA 4 AXI

CONTACT INFORMATION

PLDA
2570 North First St. , Suite 218
San Jose, CA 95131
USA
Telephone (408) 273 4528
sales@plda.com
www.plda.com

LeCroy's PCI Express® Protocol Analysis and Test Tools

Compatible Operating Systems: Windows 7/XP/Vista

Specification Compliance: PCI Express Standards: 1.1, 2.0, and 3.0

Whether you are a test engineer or firmware developer, LeCroy's Protocol Analyzers will help you quickly identify, troubleshoot and solve all your protocol problems. LeCroy works closely with industry standards groups such as the PCI-SIG®, PICMG, VITA and the Intel Embedded Communication Alliance to help developers rapidly bring to market high performance and reliable PCI Express protocol test solutions.

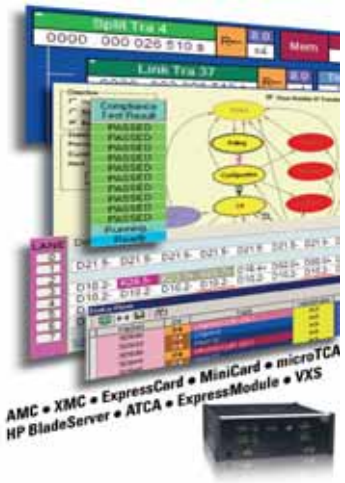
LeCroy's products include a wide range of probe connections to support VPX, XMC, AMC, ATCA, microTCA, Express Card, MiniCard, ExpressModule, HP Blade Server Modules, PCIe external cable, MidBus connectors and flexible mult-lead probes for PCIe® 1.0a, 1.1("Gen1" at 2.5GT/s) , PCIe 2.0("Gen 2" at 5 GT/s) and PCIe 3.0("Gen 3" at 8 GT/s).

The high performance SummitTM T3-16 Protocol Analyzer features the new PCIe extensions for NVMHCI 1.0(SSD devices), SR-IOV, MR-IOV, and in-band logic analysis.

LeCroy offers a complete range of protocol test solutions, including analyzers, exercisers, protocol test cards, and physical layer testing tools that are certified by the PCI-SIG for ensuring compliance and compatibility with PCI Express specifications.

FEATURES & BENEFITS

- **One button protocol error check.** Lists all protocol errors found in a trace. Great starting point for beginning a debug session.
- **Flow control screen** that quickly shows credit balances for root complex and endpoint performance bottlenecks. Easily find out why your add-in card is underperforming on its benchmarks.
- **LTSSM state view screen** that accurately shows power state transitions with hyperlinks to drill down to more detail. Helps identify issues when endpoints go into and out of low power states.
- **Full power management state tracking** with LeCroy's Interposer technology. Prevents loosing the trace when the system goes into electrical idle.
- **LeCroy's Data View** shows only the necessary protocol handshaking ack/naks so you don't have to be a protocol expert to understand if root complexes and endpoints are communicating properly.
- **Real Time Statistics** puts the analyzer into a monitoring mode showing rates for any user term chosen. Good for showing performance and bus utilization of the DUT.



- **Zero Time Search** provides a fast way to search large traces for specific protocol terms.
- **Config space** can be displayed in its entirety so that driver registers can be verified.
- **Test Arcs** in the exerciser let PCie 3.0 devices to be tested at any speed and link width.

TECHNICAL SPECS

- **Analyzer**
  Lanes supported: X1,x2,x4,x8,x16
  Speeds: 2.5GT/s, 5GT/s and 8GTs
  Probes/Interposers: active and passive PCIe slot, VPX, XMC, AMC, expresscard, expressmodule, minicard, MidBus, multi-lead, and others.
  Form factor: Card, Chassis
- **Exerciser**
  Lanes supported: X1,x2,x4,x8,x16
  Speeds: 2.5GT/s, 5GT/s, 8GT/s
  Emulation: root complex and endpoint emulation
- **Protocol Test Card**
  Speeds: 2.5GT/s and 5GT/s operation
  Tests: Add-in-card test
  BIOS Platform Test
  Single Root IO Virtualization Test

APPLICATION AREAS

Mezzanine Boards, Add-in Cards, Host Carrier Systems, System Boards, Chips

CONTACT INFORMATION

LeCroy

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Santa Clara, CA, 95054
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1 800 909-7211 Toll Free
1 408 727-6622 Fax
sales@catc.com
http://www.lecroy.com

Connect Tech Inc.

PCI Express Solutions – Connect Tech Inc.

Supported PCI Express Standards: PCI Express x1, x4, x8, x16 compatible, PCI/104-Express, PCIe/104

OS Support: Windows 7/2000/XP/XPe/Server2003/CE/Vista, Linux, QNX

Bus Interface: PCI Express

Connect Tech delivers PCI Express solutions that are ideally suited for the demanding needs of users in the industrial and embedded markets. Our PCI Express products include single board computers, multi-port serial cards, and a range of development tools and adapters including burn-in racks and dump switch cards.

BlueStorm/Express Multi-Port Serial Cards
BlueStorm/Express products are available with 2 to 16 serial ports; low profile and standard height designs are available. The BlueStorm/Express line offers RS-232/422/485 connectivity; compatible with any x1, x4, x8 or x16 PCIe slot. Choose from:

- **BlueStorm/Express:** Standard height, 2, 4, 8 or 16 ports RS-232/422/RS-485
- **BlueStorm/Express Opto:** Standard height, 4 ports RS-232/422/485, with 3kV optical isolation on all 4 ports
- **BlueStorm/Express Opto (1kV):** Standard height, 8 ports RS-232/422/485, with 1kV optical isolation on 4 of 8 ports
- **BlueStorm/Express LP:** Low profile, 8 ports RS-232/422/485, with surge suppression
- **BlueStorm/Express LP Opto:** Low profile, 2 ports RS-232/422/485, with 3kV optical isolation on both ports
- **BlueStorm/Express Isolated:** Standard height, 8 ports RS-232, with 2kV optical isolation on all 8 ports (3kV on board)
- **BlueStorm/Express 8/16 Port RS-232:** Standard height, 8 or 16 ports RS-232

PCI Express Dump Switch Card
The PCI Express Dump Switch Card is ideal for the software developer. Should a system lock-up occur, the push of the dump switch button forces an NMI/SERR triggering a crash dump or drops execution into your operating system's debugger.

PCI Express Burn-in Rack
Burn in up to 10 cards simultaneously with the PCIe Burn-in Rack, without the need for a dedicated computer system.

PCI Express to PCIe/104 Adapter
The PCI Express to PCIe/104 Adapter allows users to install a PCIe/104 or PCI/104-Express card into a standard PCI Express slot.

FEATURES & BENEFITS

- **BlueStorm/Express Multi-Port Serial Cards:** Choose up to 16 ports, RS-232/422/485, low profile and standard height models
- **PCI Express Dump Switch Card:** An ideal debugging tool for Software Engineers
- **PCI Express Burn-in Rack:** Accommodate up to 10 PCIe cards
- **PCI Express to PCIe/104 Adapter:** x1 lane PCI Express card edge for installation in any slot width

TECHNICAL SPECS

- Multi-Port Serial Cards are compatible with x1, x4, x8 and x16 PCIe slots
- Lifetime warranty and free technical support
- Optional optical isolation
- Custom Design Services: Connect Tech will work with you to implement a solution that will meet your needs.

AVAILABILITY

Immediate.

APPLICATION AREAS

Industrial Automation, Material Handling, Transportation, Military and Aerospace, Test & Measurement, Point of Sale.

CONTACT INFORMATION

Connect Tech

Connect Tech Inc.
42 Arrow Road, Guelph, ON Canada N1K 1S6
Telephone: 519.836.1291
North America: 800.426.8979
Fax: 519.836.4878
Web site: www.connecttech.com
Email: sales@connecttech.com

PCIe/104 and PCI/104-Express Solutions – Connect Tech Inc.

Supported PCIe/104 and PCI/104-Express Standards: PCI/104-Express, PCIe/104

OS Support: Windows 7/2000/XP/XPe/Server2003/CE/Vista, Linux, QNX

Bus Interface: PCIe/104 and PCI/104-Express

Connect Tech delivers PCIe/104 and PCI/104-Express solutions that are ideally suited for the demanding needs of users in the industrial and embedded markets. Our products include single board computers, multi-port serial cards, development tools and adapters.

Xtreme/CPU - PCI/104-Express Single Board Computer
Connect Tech's PCI/104-Express Single Board Computers offer a variety of embedded processor solutions including Intel Atom, Freescale i.MX51, TI OMAP and NVIDIA Tegra. Our single board computers give instant access to a full range of PCI/104-Express peripherals from a rapidly growing eco-system including FPGA solutions, multi-port serial, frame grabbers and more. Xtreme/CPU solutions are modular and completely scalable, with access to the most current embedded processers that are easily upgradable to accommodate future generations of Intel Atom processors, such as Tunnel Creek, or ARM based processors, such as Cortex A8. Xtreme/CPU solutions conveniently provide on-board connectors allowing for instant access to a variety of features including 2x SATA, 1x Gigabit Ethernet, VDS, 4x USB 2.0, VGA Video and 2x RS-232, 2 x RS-422/485.

Xtreme/104-Express Serial Board
The Xtreme/104-Express serial board is compatible with PCIe/104 and PCI/104-Express stacks. It offers 8 x RS-232/422/485 serial ports.

Xtreme/104-Express Opto Serial Board
The Xtreme/104-Express Opto serial board offers 8 x RS-232/422/485 serial ports, along with 3 kV optical isolation to protect your industrial and embedded applications.

PCIe/104 to PCI Express Bottom Stacking Adapter
This adapter allows users to install any x1, x4, x8 or x16 lane PCI Express card into a PCIe/104 or PCI/104-Express stack down configuration.

PCIe/104 to PCI Express Top Stacking Adapter
This adapter allows users to install any x1, x4, x8 or x16 lane PCI Express card into a PCIe/104 or PCI/104-Express stack up configuration.

FEATURES & BENEFITS

- Xtreme/CPU: embedded processor options include Intel Atom, Freescale i.MX51, TI OMAP and NVIDIA Tegra
- Xtreme/104-Express Serial Board: up to 16 ports, RS-232/422/485, low profile and standard models
- Xtreme/104-Express Opto Serial Board: 8 ports, RS-232/422/485, 3 kV optical isolation
- PCIe/104 to PCI Express Bottom Stacking or Top Stacking Adapters: supports any x1, x4, x8 or x16 lane PCI Express card

TECHNICAL SPECS

- Single Board Computers provide on-board connectors allowing for instant access to features including 2x SATA, 1x Gigabit Ethernet, VDS, 4x USB 2.0, VGA Video and 2x RS-232, 2 x RS-422/485
- Lifetime warranty and free technical support
- Custom Design Services: Connect Tech will work with you to implement a solution that will meet your needs.

AVAILABILITY

Immediate.

APPLICATION AREAS

Industrial Automation, Material Handling, Transportation, Military and Aerospace, Test & Measurement, Point of Sale.

CONTACT INFORMATION

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Web site: www.connecttech.com
Email: sales@connecttech.com

Innovative Integration

X5 Family PCI Express XMC Modules

OS Support: Windows, Linux,and VXWorks/Wind River

Bus Interface: PCI Express, adapters for PCI, cPCI, & VPX

The X5 module family integrates high performance I/O with Xilinx Virtex5 FPGA computing core on 75x150mm module (IEEE1386) with a PCI Express interface. The Virtex5 SXT FPGA provides up to 640 DSP48 elements combined with memory that is critical to implementing efficient signal processing algorithms and data acquisition.

Innovative's unique Velocia architecture provides up to 1 GB/s data streaming to the host that is flexible & extensible for all types of applications. It's fast and easy to use—allowing you to concentrate on your application work because it handles all the data flow and routing. You can freely mix high rate data streams with control and status making it easy to adapt to you application, yet still achieve the full GB/s data rate capabilities of the PCIe interface.

All X5 modules are architected to deliver high data throughput to the Host, along with the flexibility of user-customizable FPGA signal processing. Board specific analog or digital I/O flows directly into the user-configurable Xilinx 5 logic device. The supplied stock logic functionality allows the board to be used out-of-the-box as a high-speed I/O board in which the large onboard DDR2 DRAM is configured as an enormous virtual FIFO data buffer. The QDR SRAM interface is a very high-speed local cache for custom algorithms running within the FPGA. Download pricing and data sheets from www.innovative-dsp.com

FEATURES & BENEFITS

- Ultra-fast signal capture, generation & co-processing - Spartan 3 & Virtex-5 FPGA, huge DDR/QDR memory, multi-lane PCI Express with a private J16 user I/O port. Excellent choice for SDR, signal intelligence, RADAR, radio test equipment.
- X5-210M: PCI Express XMC Module with Four 250 MSPS 14-bit A/Ds, Virtex5 FPGA, and DDR2/QDR-II Memory
- X5-G12: PCI Express XMC Module with Dual channel 1 GSPS,12-bit Digitizer, Virtex5 FPGA and 512MB Memory
- X5-400M PCIe XMC Module - Two 400 MSPS, 14-bit TI ADS5474 ADCs and Two 500 MSPS, 16-bit DACs, Virtex5 FPGA and 512 MB Memory
- X5-GSPS: PCI Express XMC Module with Two 8-bit National ADC08D1500 A/Ds, Virtex5 FPGA and 512 MB Memory

TECHNICAL SPECS

- 400 MSPS, 14-bit A/D channels
  Two 500 MSPS, 16-bit DAC channels
  +/-1V, 50 ohm, SMA inputs and outputs
- Xilinx Virtex5, SX95T FPGA
  512 MB DDR2 DRAM
  4 MB QDR-II SRAM
- 8 Rocket IO private links, 2.5 Gbps each
  1 GB/s, 8-lane PCI Express Host Interface
- Power Management features
  XMC Module (75x150 mm)
  PCI Express (VITA 42.3)
- Ruggedization Levels for Wide Temperature Operation
  Adapters for VPX, Compact PCI, Desktop PCI and Cabled PCI Express System

AVAILABILITY

Shipping

APPLICATION AREAS

- Wireless Receiver and Transmitter
- WLAN, WCDMA, WiMAX front end
- RADAR
- Electronic Counter Measures (ECM)
- Electronic Warfare
- High Speed Data Recording and Playback
- High speed servo controls
- Spectral Analysis
- IP development

CONTACT INFORMATION

Innovative Integration
2390 Ward Avenue
Simi Valley, CA 93065
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805-578-4260 Telephone
805-578-4225 Fax
sales@innovative-dsp.com
www.innovative-dsp.com

X6-RX

OS Support: Windows, Linux,and VXWorks/Wind River

Bus Interface: natively xmc/pmc adapters to VPX, cPCI, PCI, PCI Express

The X6-RX is a flexible receiver that integrates IF digitizing with signal processing on a PMC IO module. Up to 24 configurable receiver channels with a powerful Xilinx Virtex 6 FPGA signal processing core, & high performance PCI Express/PCI host interface. With the X6-RX, IF recorders can log both the digitized raw data & channels real-time sustaining rates over 2 GB/s.

The X6-RX features four, 16-bit 160 MSPS A/Ds with dual digital downconverters (DDC). IF frequencies of up to 300 MHz are supported. The sample clock is from either a low-jitter PLL or external input. Multiple cards can be synchronized for sampling & downconversion.

A Xilinx Virtex6 SX315T (LX240T at initial release) with 4 banks of 128MB DRAM provide a very high performance DSP core with over 2000 MACs (SX315T). The close integration of the analog IO, memory & host interface with the FPGA enables real-time signal processing at extremely high rates.

Onboard DDC ASIC device, connected directly to the FPGA, provides up to 24 narrowb &/or 8 wideb & channels with input from two A/D channels. The DDC performs complex or real downconversion, with flexible controls for mixing, filtering, decimation, output formats & data rates. Channels can be synchronized to support beam forming or frequency hopped systems.

Power is less than 15W for typical operation. VITA 20 conduction cooling is used with a heat-spreader & sink are Ruggedization levels for wide-temperature operation & conformal coating are supported.

FEATURES & BENEFITS

- Four 160 MSPS, 16-bit A/D channels
  Down-Converter ASIC supporting up to 24 Narrowband or 8 Wideband Channels
  +/-1V, AC-Coupled, 50 ohm, SMA inputs
- Xilinx Virtex6 SX315T/SX475T or LX240T
  4 Banks of 128MB DRAM
  Ultra-low jitter programmable clock
- x8 PCI Express Gen2, providing 2 GB/s sustained transfer rates
  PCI 32-bit, 66 MHz with P4 to Host card
- PMC/XMC Module (75x150 mm)
  15W typical
  Conduction Cooling per VITA 20

- Ruggedization Levels for Wide Temperature Operation Adapters for VPX, Compact PCI, desktop PCI and cabled PCI Express systems

TECHNICAL SPECS

- Available XMC carrier adapters offer conduction & convection cooling & are available for a range of interfaces including Desktop PCI, Desktop PCI Express, Cabled PCI Express, CompactPCI, & PXI/PXI Express.
- Extremely versatile, easily adapted for use in virtually any type of system.
  The X6-RX is also readily installed into Innovative Integration's eInstrument Embedded PC, SBC-ComEx Single-Board Computer, & Andale Data Loggers.
- PCI gen 2 to 24 Megabytes per second.
  200 fS clock jitter
- 15 watt nominal power dissapation!
- Military rugged versions available.

AVAILABILITY

Shipping

APPLICATION AREAS

- Wireless Receiver
- WLAN, WCDMA, WiMAX front end
- RADAR
- Medical Imaging
- High Speed Data Recording and Playback
- IP Development

CONTACT INFORMATION

Innovative Integration
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805-578-4225 Fax
sales@innovative-dsp.com
www.innovative-dsp.com

VersaLogic Corp.

Komodo (VL-EPICs-36)

OS Support: Compatible with most x86 operating systems including Windows, Windows Embedded, Linux, VxWorks, and QNX.

Bus Interface: SUMIT (PCIe, USB, LPC, SPI, SMBus), PC/104 (ISA), SPX

Based upon the EPIC-sized industry standard footprint, the Komodo features the SUMIT expansion interface as defined by the Small Form Factor Special Interest Group (SFF-SIG). This provides OEMs with a stackable multi-board expansion interface that supports both high- and low-speed signals. This simplifies adding both standard and custom I/O boards to the system. The Komodo expansion interfaces include PCIe, USB, LPC, SPI, SMBus, as well as ISA bus support for PC/104 modules.

The combination of Intel's dual core processor, along with its companion chipset, provide the majority of the Komodo's features including high-speed video with LVDS and analog VGA output, four USB 2.0 ports, four serial ports, gigabit Ethernet, dual SATA interface, HD audio, and PS/2 keyboard and mouse support. The SUMIT interface provides three x1 PCIe lanes, LPC, SPI, SMBus, and four additional USB channels. The PC/104 connector provides ISA bus compatibility.

Like all VersaLogic products, this SBC is designed to support OEM applications where high reliability and long-term availability are required. From application design-in to 5+ guaranteed years of production life, the Komodo provides a durable embedded computer solution with an exceptional cost of ownership. The Komodo is manufactured and tested to the highest quality standards and is fully RoHS compliant. Customization is available, even in very low quantities.

FEATURES & BENEFITS

- SUMIT™ and PC/104™ Compatible
  Supports SUMIT and ISA expansion on an EPICô format.
- Intel® Core™2 Duo Processor
  Up to 2.26 GHz performance.
- High-performance Video
  3D video acceleration (Gen 5.0). Analog and LVDS flat panel outputs.
- Network Support
  Gigabit Ethernet with remote boot support.
- System RAM
  Up to 4 GB DDR3 RAM for system flexibility.

TECHNICAL SPECS

- USB I/O
  Four USB 2.0 ports support keyboard, mouse, and other devices.
- Device I/O
  Four serial ports, dual SATA interface, and HD audio.
- Flash Memory
  MiniBlade™ socket and eUSB interface for high-reliability flash storage.
- Extended Temperature Version
  -40° to +85°C operation for harsh environments.
- MIL-STD-202G
  Qualified for high shock/vibration environments.

AVAILABILITY

Shipping

APPLICATION AREAS

Industrial, medical, defense, and aerospace applications where performance and dependability are crucial design factors.

CONTACT INFORMATION

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Ocelot (VL-EPMs-21)

OS Support: Compatible with most X86 operating systems, including Windows, Windows Embedded, Linux, VxWorks, and QNX.

Bus Interface: SUMIT-A and SUMIT-B, ISA

Ocelot is a compact, rugged, single board computer (SBC) featuring Intel's 45 nm Atom Z5xx processor designed specifically for embedded applications. This compact SUMIT-104 SBC is ideal for defense, aerospace, medical device, robotics, and factory automation applications where high-performance, fanless, extended temperature operation is required.

Based on the industry standard PC/104 footprint, the Ocelot features the SUMIT expansion interface that provides three x1 PCIe lanes, LPC, SPI, SMBus, and four additional USB channels.

On-board features include gigabit Ethernet, three USB 2.0 ports, four serial ports, IDE interface, HD audio, ISA bus and SPX expansion interface. An IDE-based Disk on Module site offers bolt-down, bootable flash storage. The highly-integrated processor facilitates fast on-board transfers, high-speed memory access, and integrated high-performance video with flat panel LVDS or optional analog video output. A SO-DIMM socket supports up to 2 GB of DDR2 RAM.

Like all VersaLogic products, the Ocelot is designed to support OEM applications where high reliability and long-term availability are required. From application design-in to 5+ guaranteed years of production life, the Ocelot provides a durable embedded computer solution with an exceptional cost of ownership. Customization is available, even in low OEM quantities.

FEATURES & BENEFITS

- SUMIT™ and PC/104™ Compatible
  Supports SUMIT (with PCIe x1 and x4 lanes) and ISA expansion on a compact, rugged PC/104 footprint.
- Intel® Atom™ Z5xx Processor
  Up to 1.6 GHz performance with only 7W power draw.
- Fanless Operation
  No moving parts required for CPU cooling.
- Extended Temperature Version
  -40° to +85°C operation for harsh environments.
- Three USB 2.0 ports support keyboard, mouse, and other devices.

TECHNICAL SPECS

- High-performance Video
  LVDS flat panel output. Optional analog support.
- Network Support
  Gigabit Ethernet with boot ROM support.
- USB I/O
  System RAM
  Up to 2 GB socketed RAM for system flexibility.
- Device I/O
  Four serial ports, IDE interface, and HD audio.
- Disk on Module Flash Socket
  Supports removable, bootable DOM storage.

AVAILABILITY

Shipping

APPLICATION AREAS

Defense, aerospace, medical device, robotics, factory automation.

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PCIe: A Developer's Challenge; An Inventor's Enabler

By Alex Goldhammer, Strategic Marketing Manager PCIe and Aurora, Xilinx Inc.

Intel has done a fabulous service for the electronics industry over the last two decades by enabling PCI and subsequent PCI Express (PCIe) interconnect standards. The PCI standards, managed by the PCI-SIG, have helped an enormous amount of companies mix and match their electronic systems to create an even more enormous amount of products that have profoundly impacted our daily lives. I anticipate that the coming PCIe Gen3 standard will rapidly accelerate the creation of a multitude of new products across a growing number of vertical markets, all interconnected via 10 Gigabit Ethernet, 40 Gigabit Ethernet and even 100 Gigabit Ethernet.

"With the introduction of each new generation of the interconnect standard, new challenges arise for the companies creating devices that will comply with the standard."

But with the introduction of each new generation of the interconnect standard, new challenges arise for the companies creating devices that will comply with the standard. PCIe Gen2 and Gen3 are certainly no exception.

The biggest advantage of moving to any new PCI Express generation is that each new one typically doubles the speed and bandwidth over the previous generation. This means remarkable things for each new generation of devices but can be quite a challenge for the folks designing systems that comply with the standard.

For IP and device manufacturers, this means each generation of their IC or core's internal data path must also double. This can be a huge challenge for companies creating next generation devices but even more so for IP companies or companies that maintain their own IP libraries. In making their cores comply with the standard, they must also ensure their cores remain efficient but stay essentially the same size when implemented in silicon. Creating compliant devices and IP is further complicated by the fact that the PCI-SIG and other companies are constantly coming up with new optional features above and beyond the base standard.

On the IC side, companies wishing to create products that comply with each new generation of PCIe must also deal with ever more complex link training and state machines. The link training is the automatic mechanism where systems linked via PCIe negotiate lane widths and lane speeds. These operate autonomously (without need for user intervention) and must be extremely robust for reliable system performance.

With PCIe Gen3, data rates increased to 8Gbps and the encoding has changed to 128b/130b with scrambling. Unfortunately, this isn't the same encoding used for PCIe Gen1 and Gen2. Thus companies wishing to comply with the standard must ensure their systems can easily switch encoding from Gen3's128b/130b to a more industry standard 8b/10b used in Gen1 and Gen2 (PCIe Gen3 must also support Gen1 and Gen2 data rates). In addition to requiring encoding switches, Gen3 requires chips to include transceivers that support complex decision feedback equalization (DFE). Many companies will need to add DFE support to their devices, if they don't have them already.

But from a developer's perspective, it isn't all bad news. Both PCI Gen2 and USB 3.0 protocols are wonderful in that that they use the Intel PIPE 2.0 specification as the basis for the internal interface between the Protocol Layers and the gigabit transceivers (PHY). From a gigabit transceiver development perspective this helps engineers reuse a lot of the verification and testing infrastructure needed for transceivers. If this trend continues, it will also hopefully reduce the numbers of different transceivers in the market, making transceivers easier to test and validate while increasing reliability. This will seemingly help companies like Xilinx bring products based on PCIe Gen3 and subsequent generations to market even sooner.

"Creating compliant devices and IP is further complicated by the fact that the PCI-SIG and other companies are constantly coming up with new optional features above and beyond the base standard."

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